

FIG. 1

FIG. 2

FIG. 3

FIG. 4

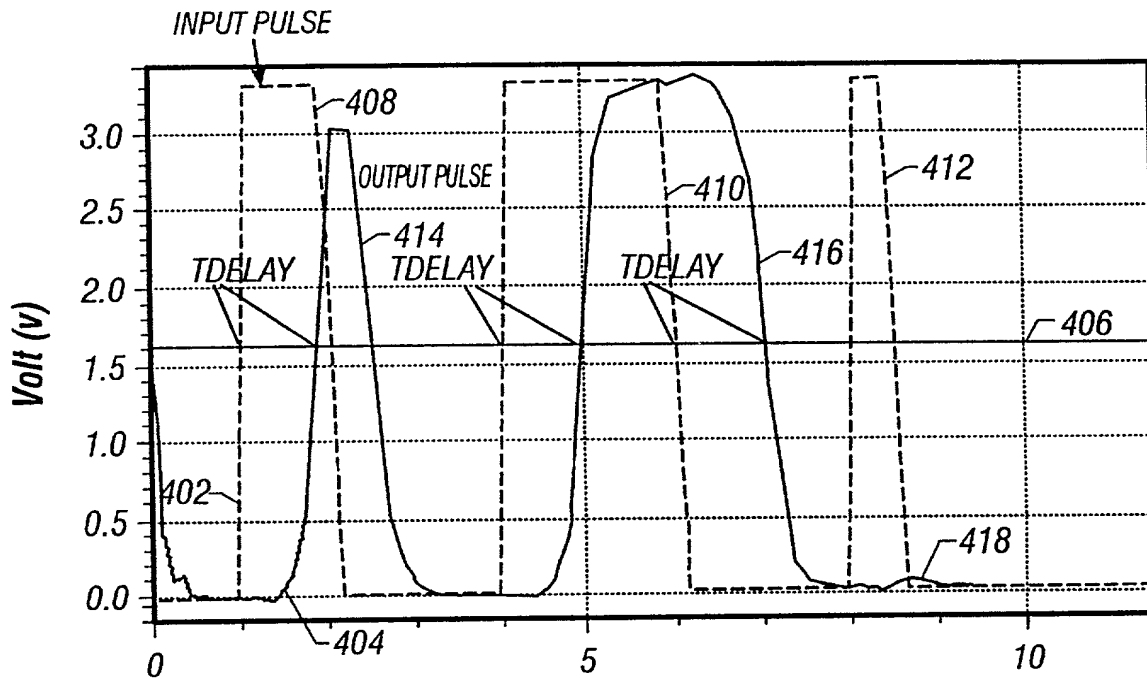


FIG. 4

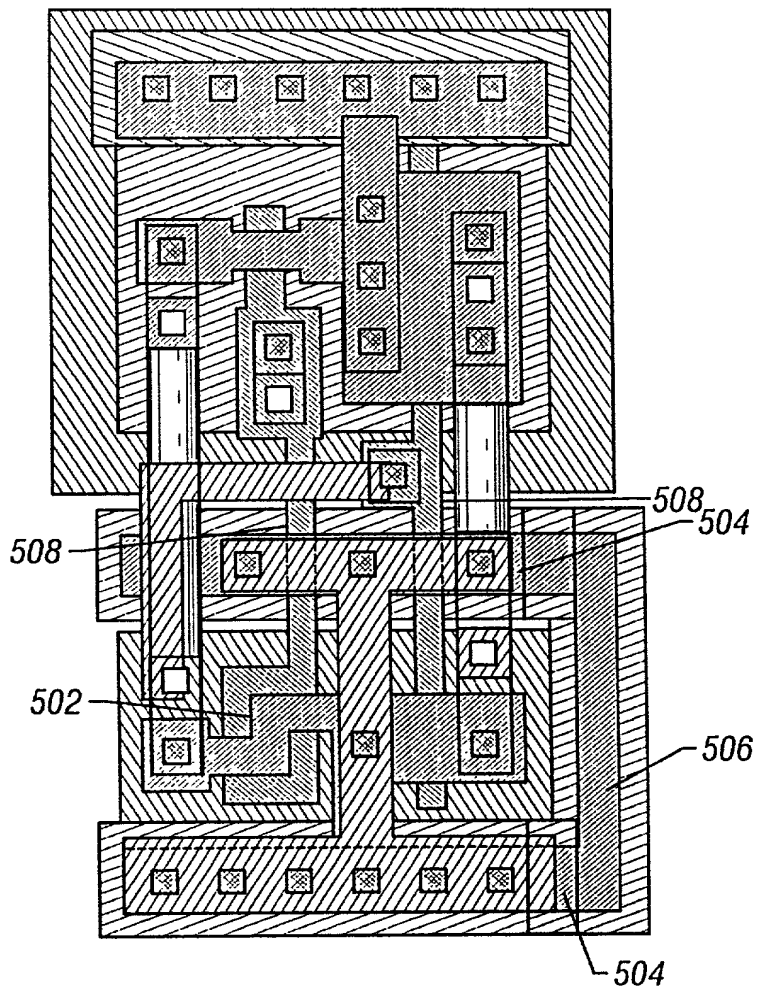


FIG. 5A

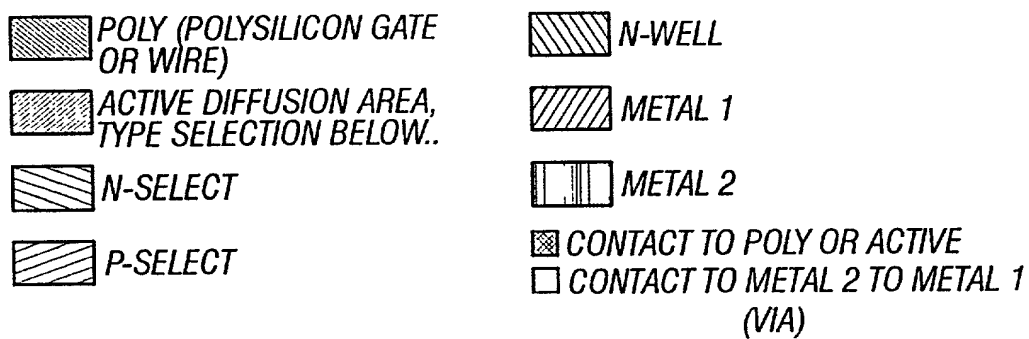


FIG. 5B

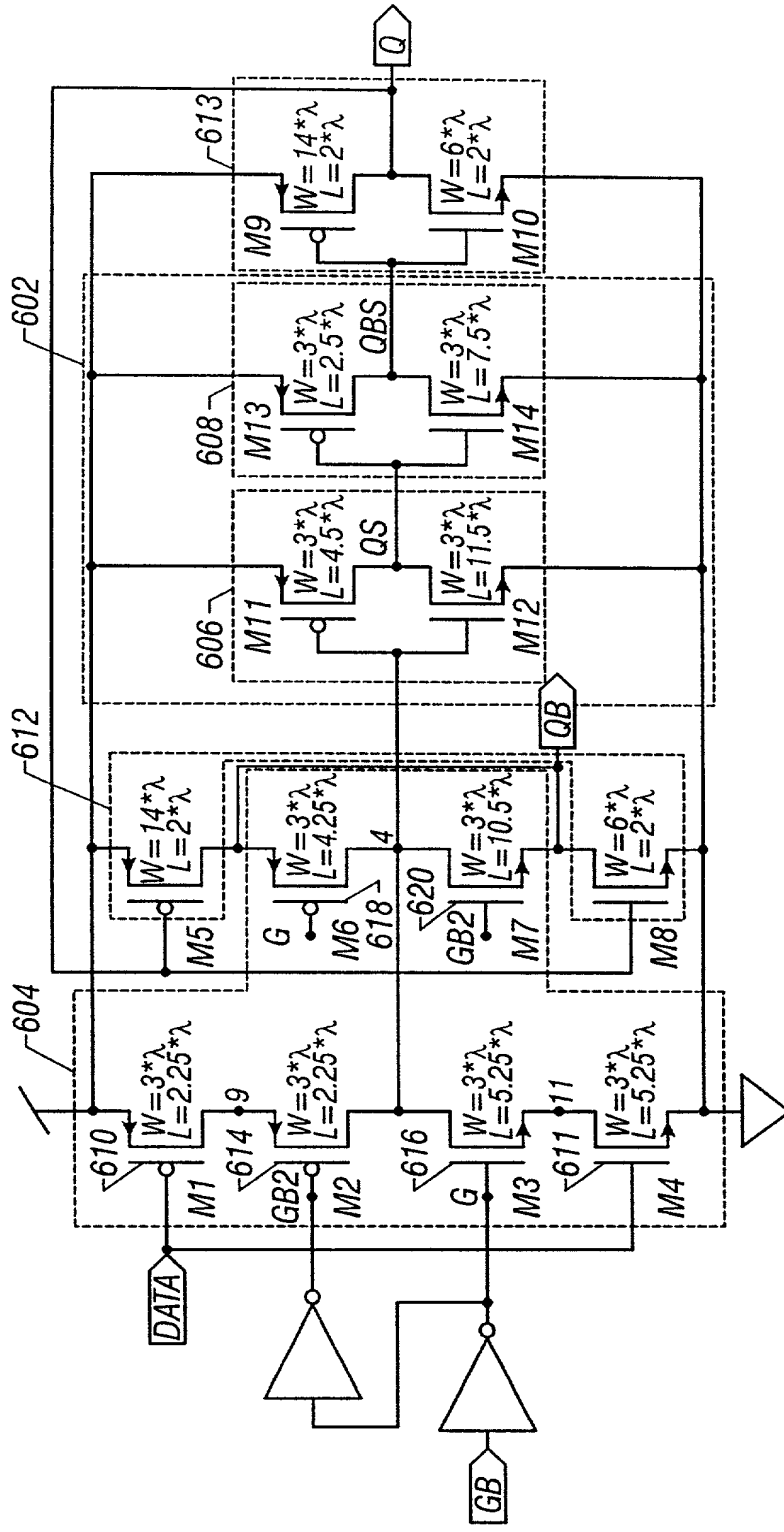


FIG. 6

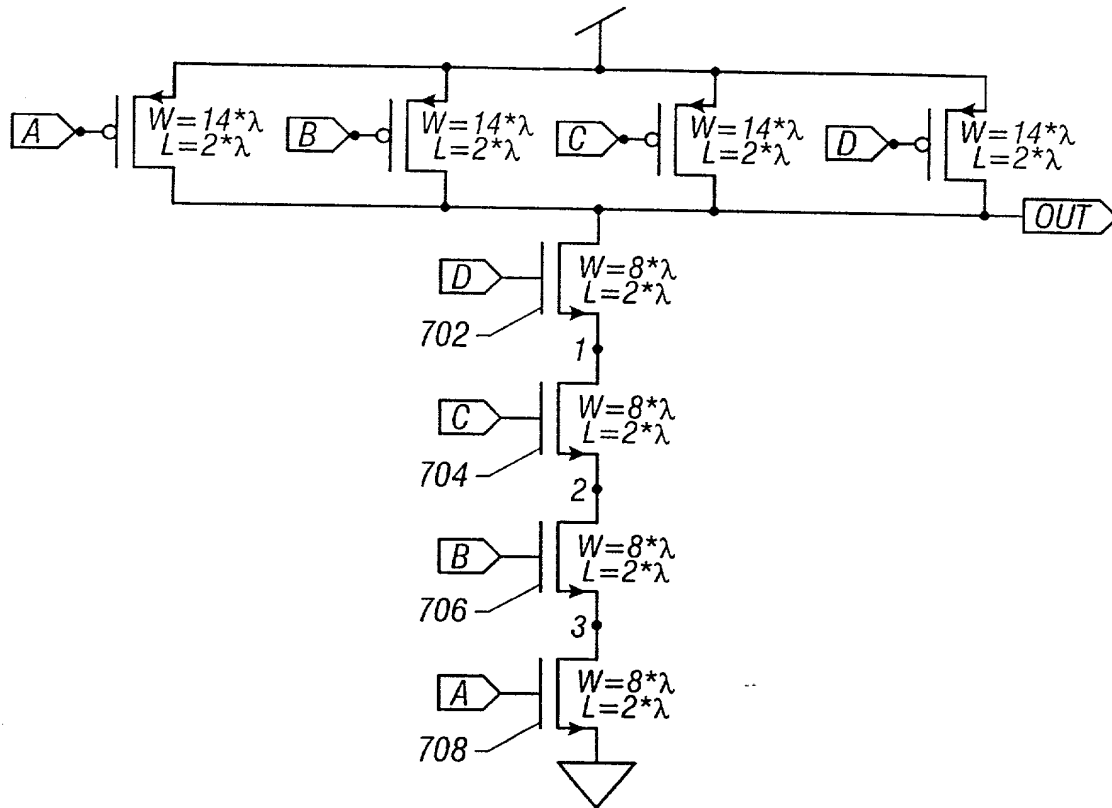


FIG. 7A

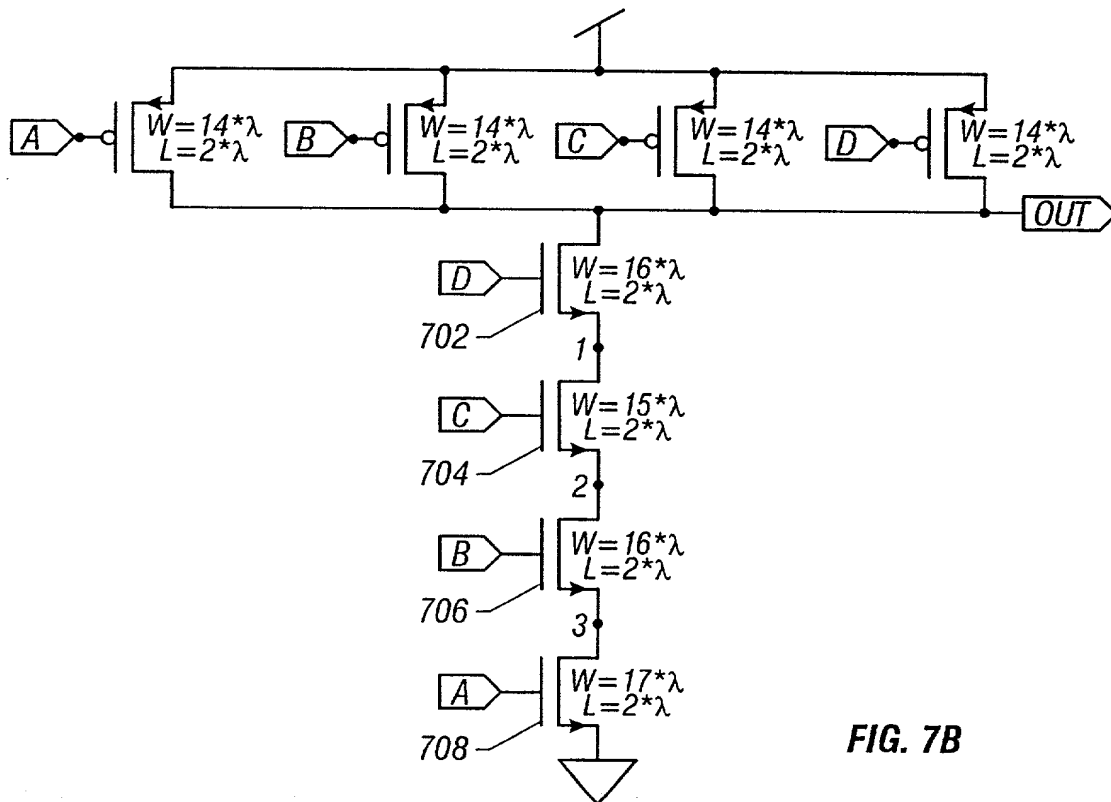


FIG. 7B

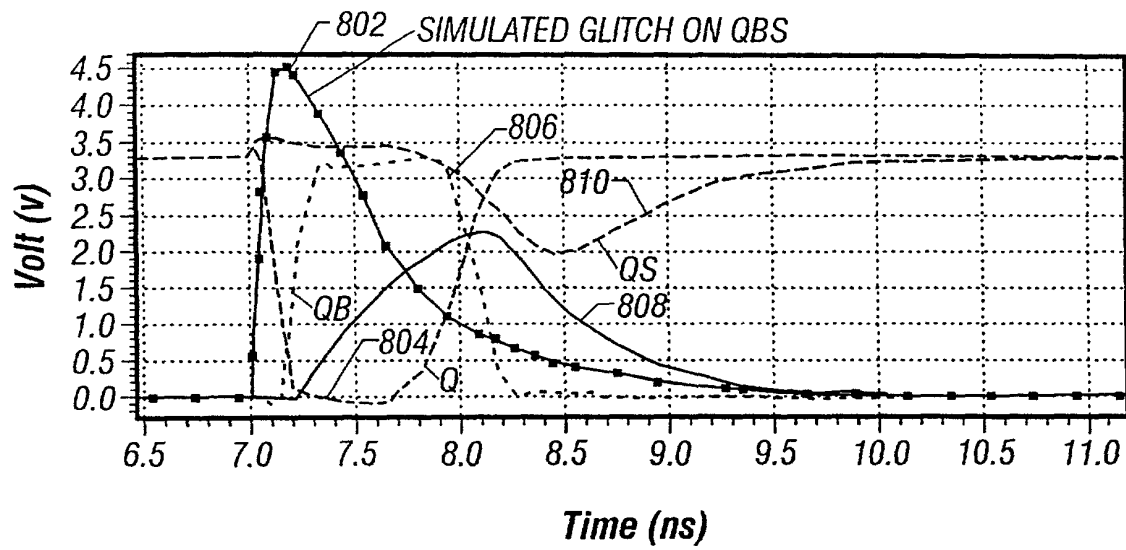


FIG. 8

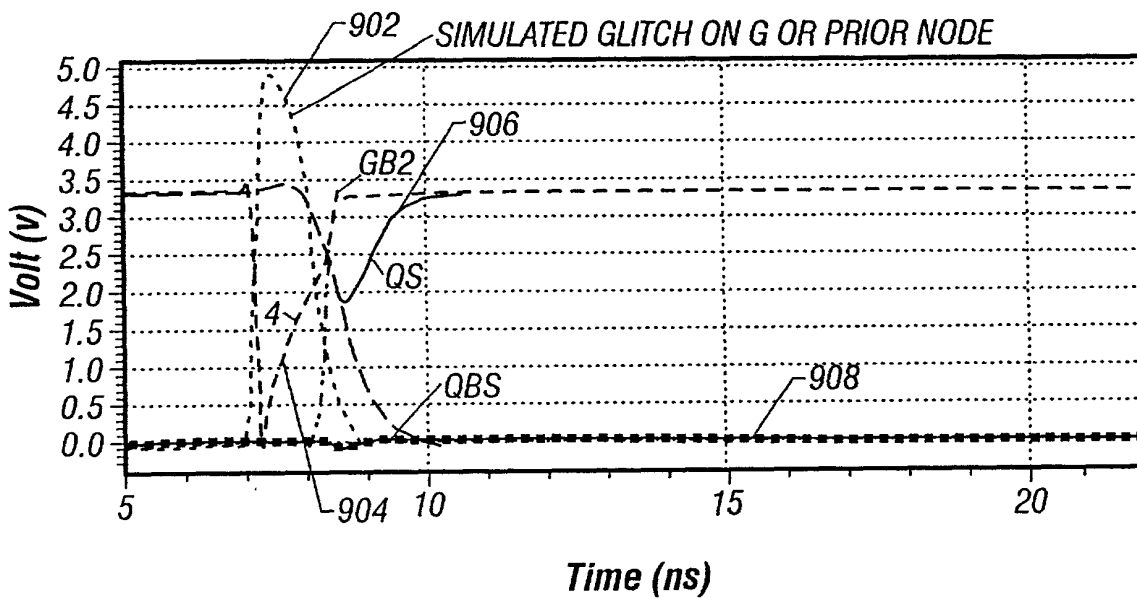


FIG. 9

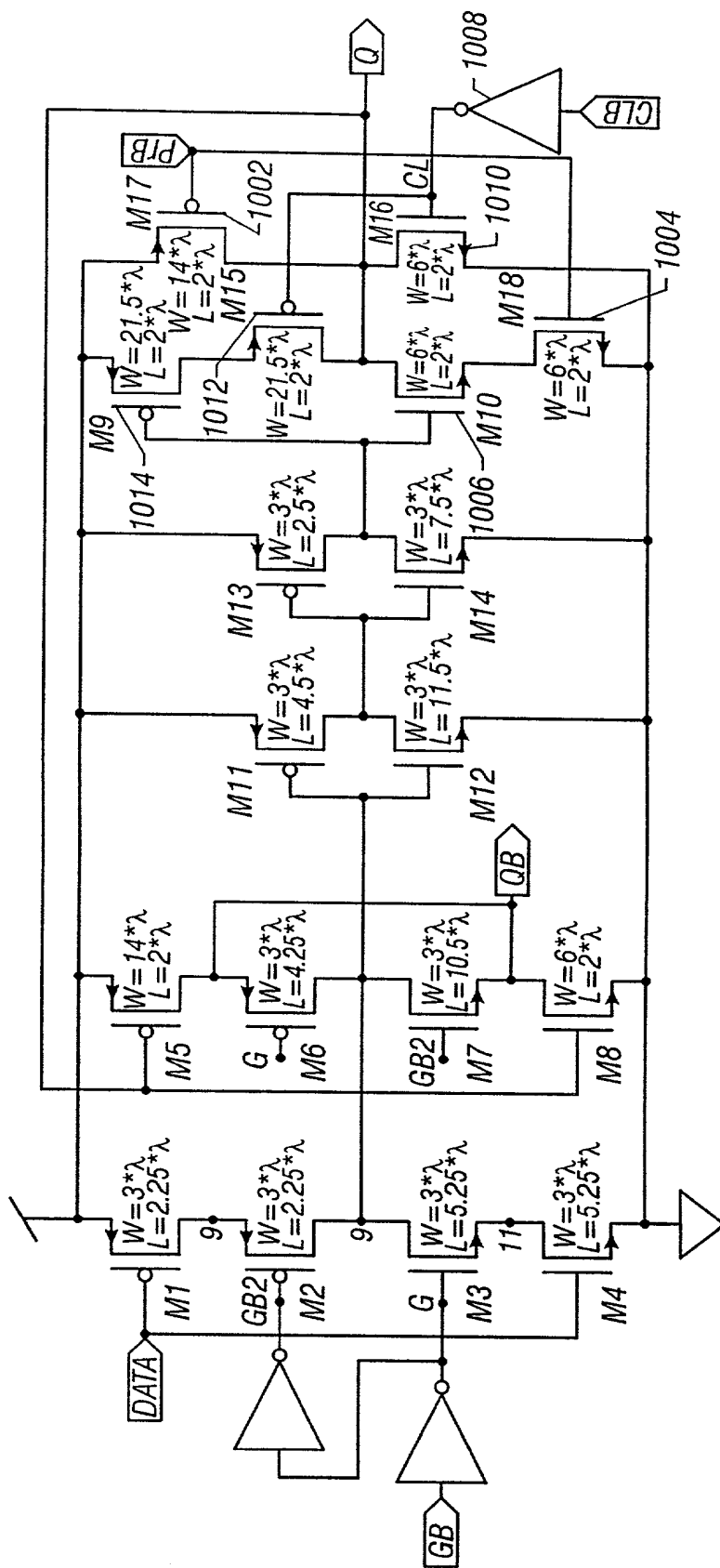


FIG. 10

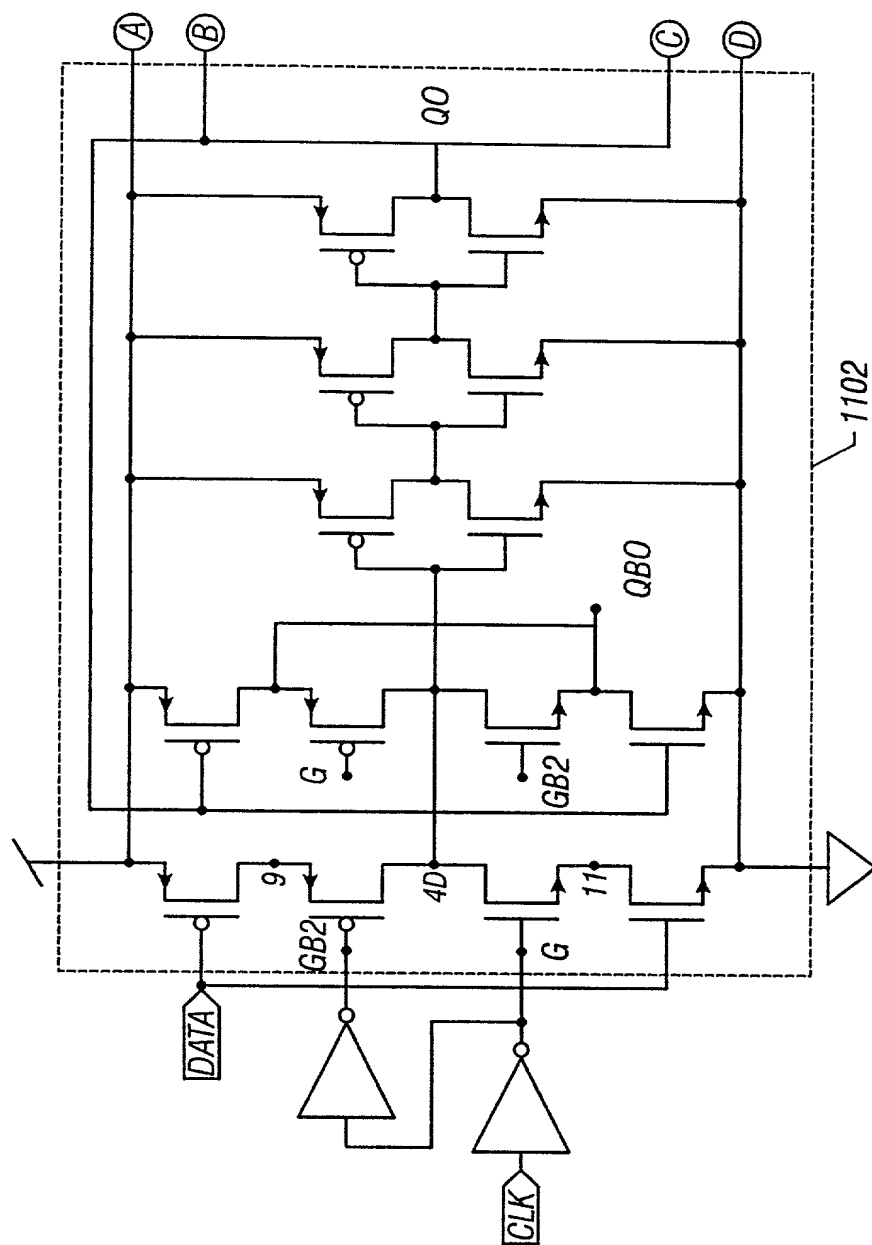


FIG. 11A

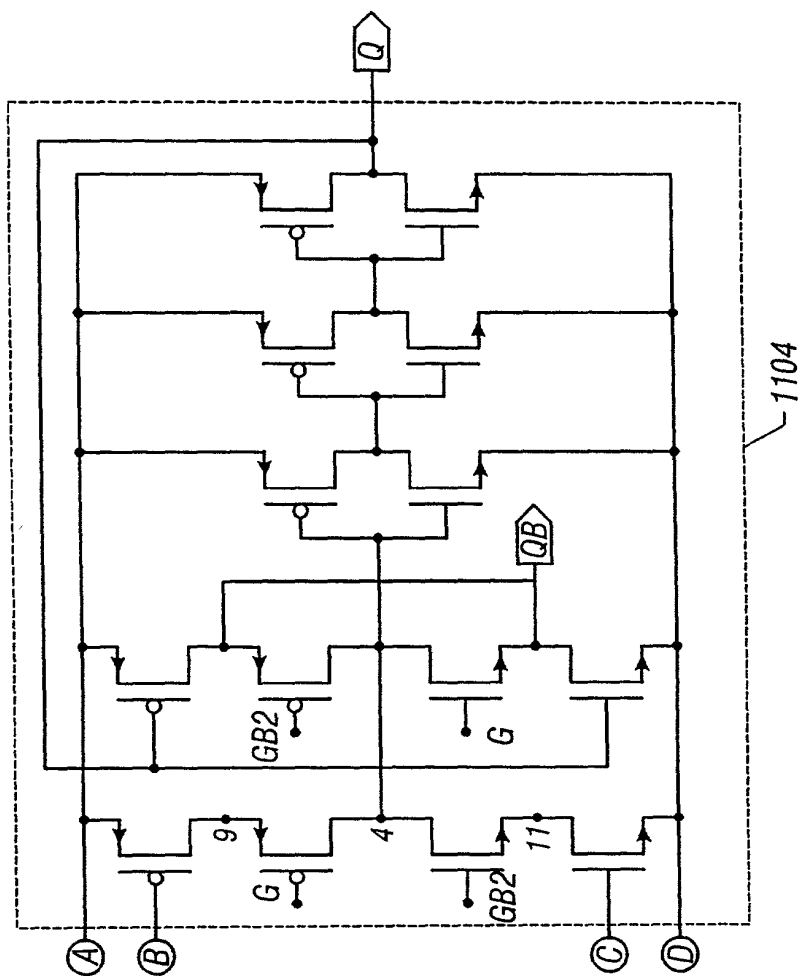


FIG. 11B

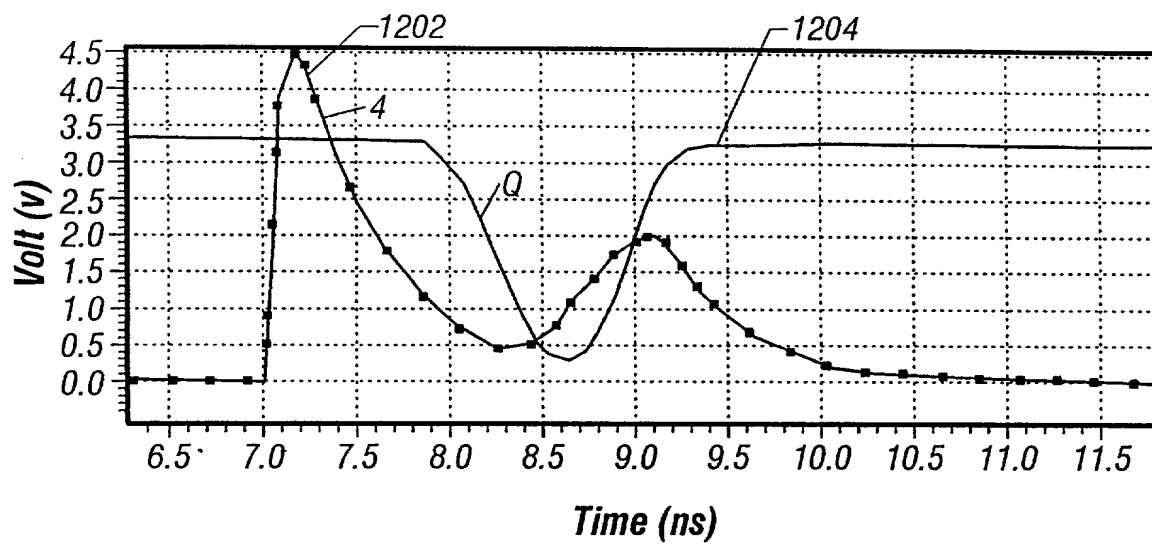


FIG. 12

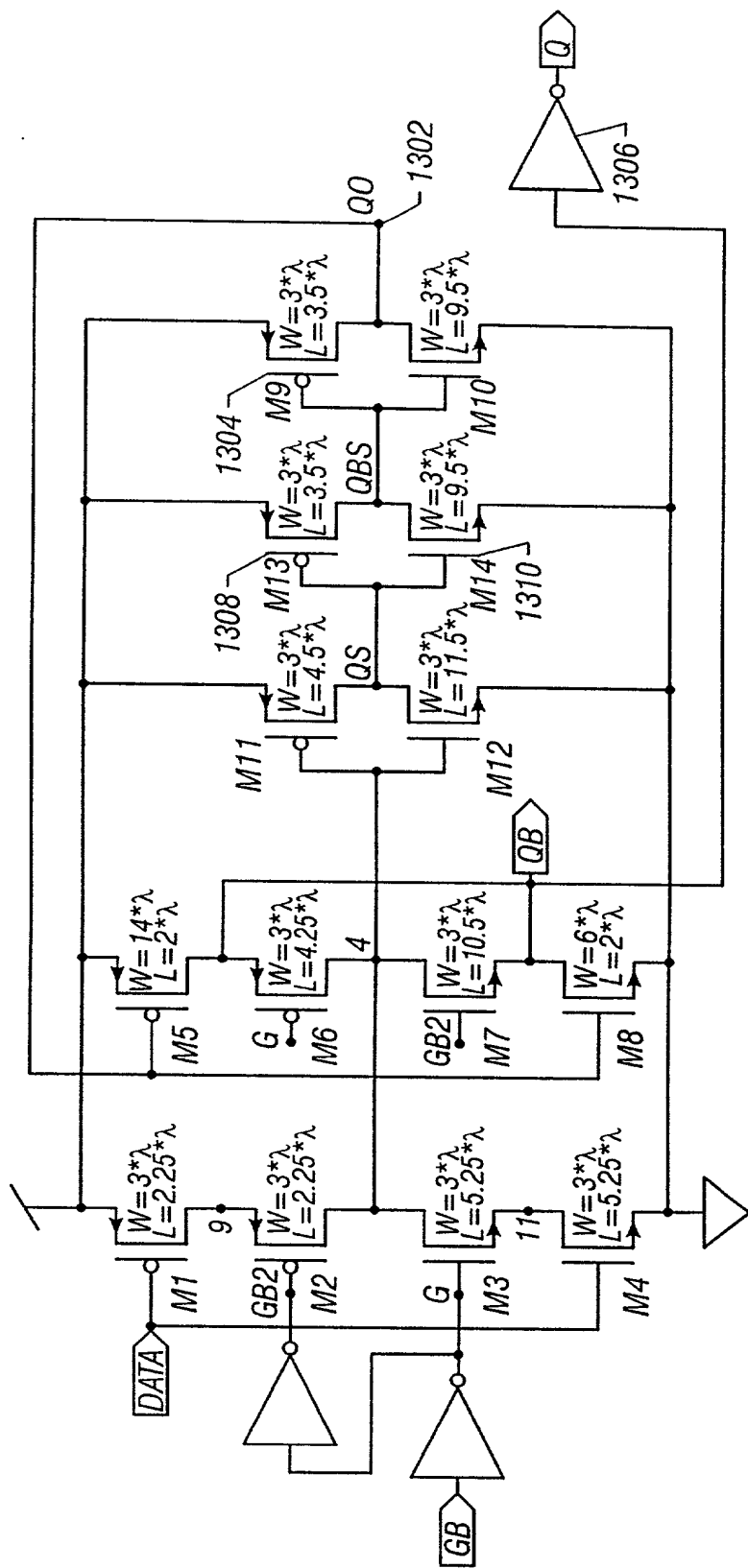


FIG. 13

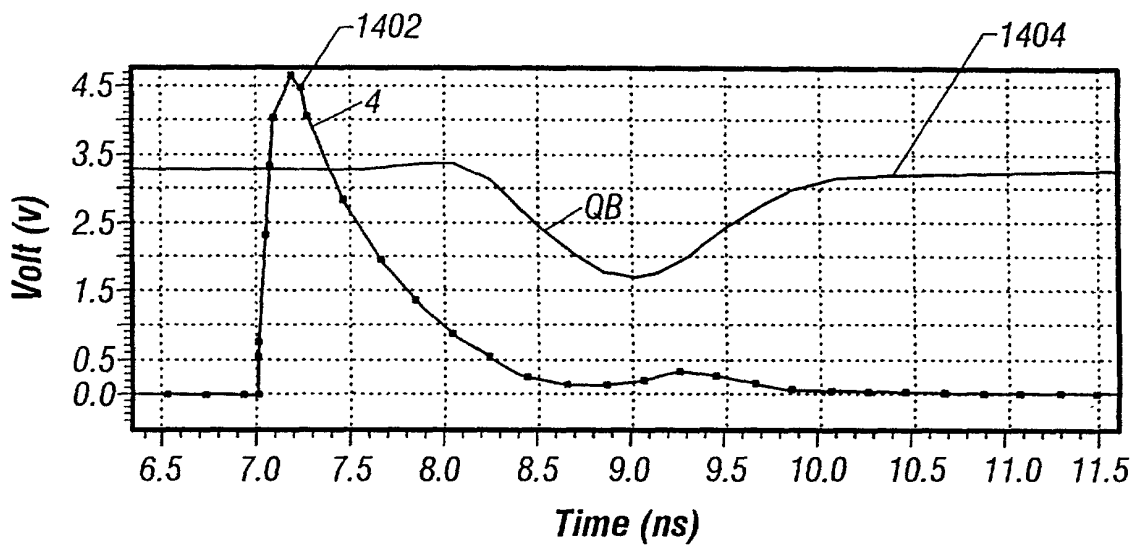


FIG. 14

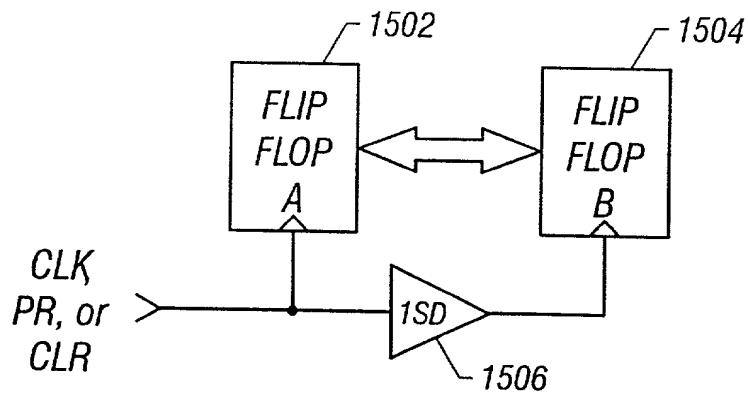


FIG. 15

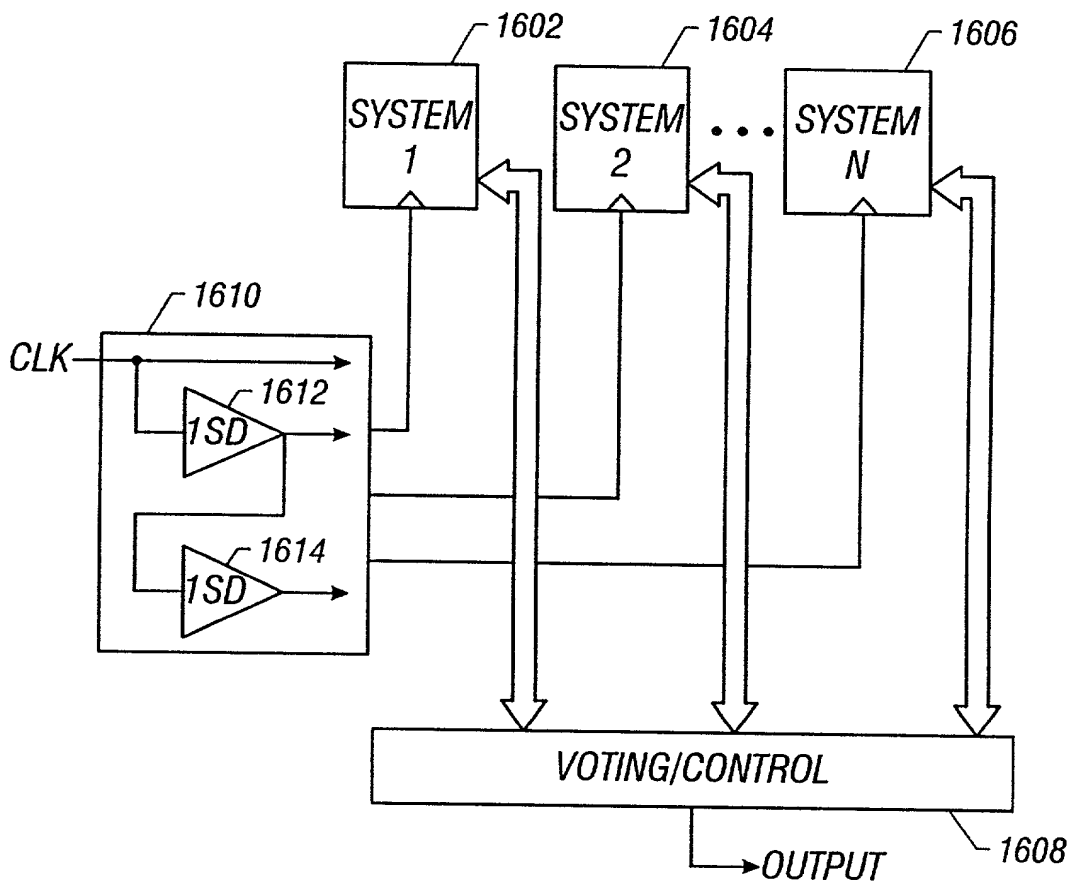


FIG. 16

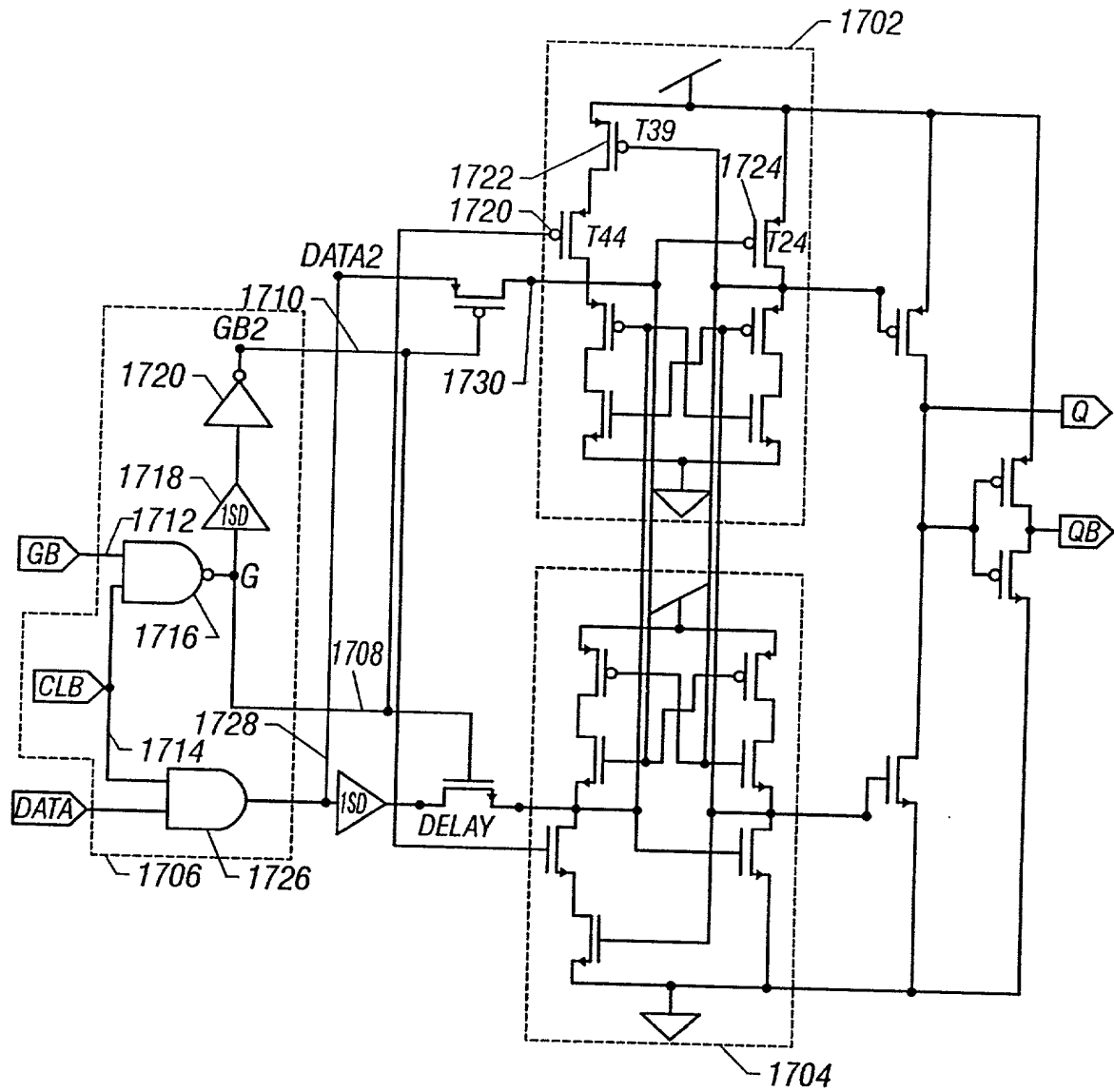
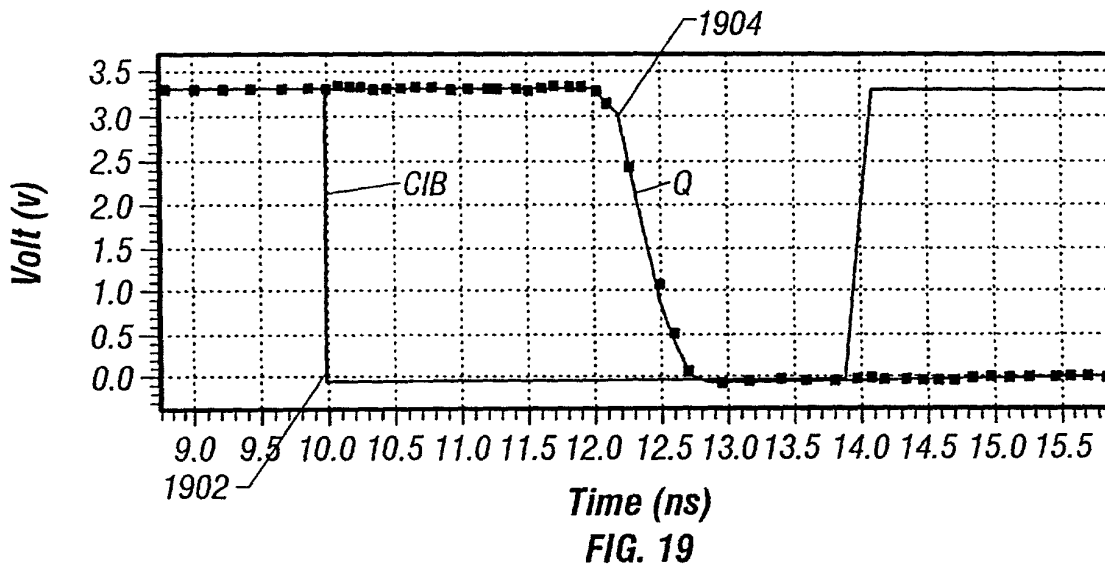
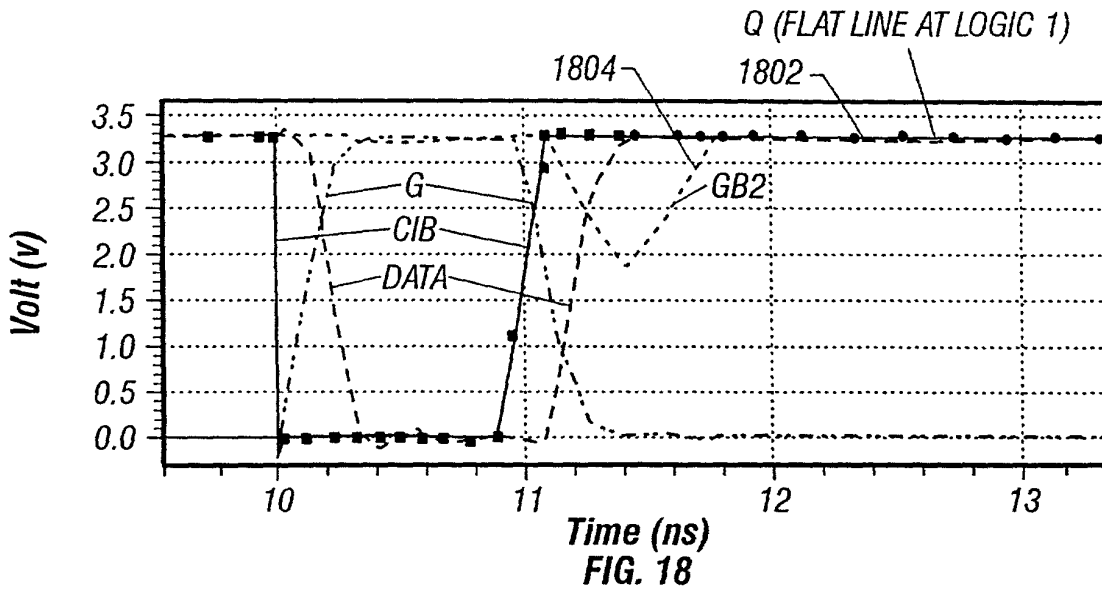


FIG. 17

FIG. 18



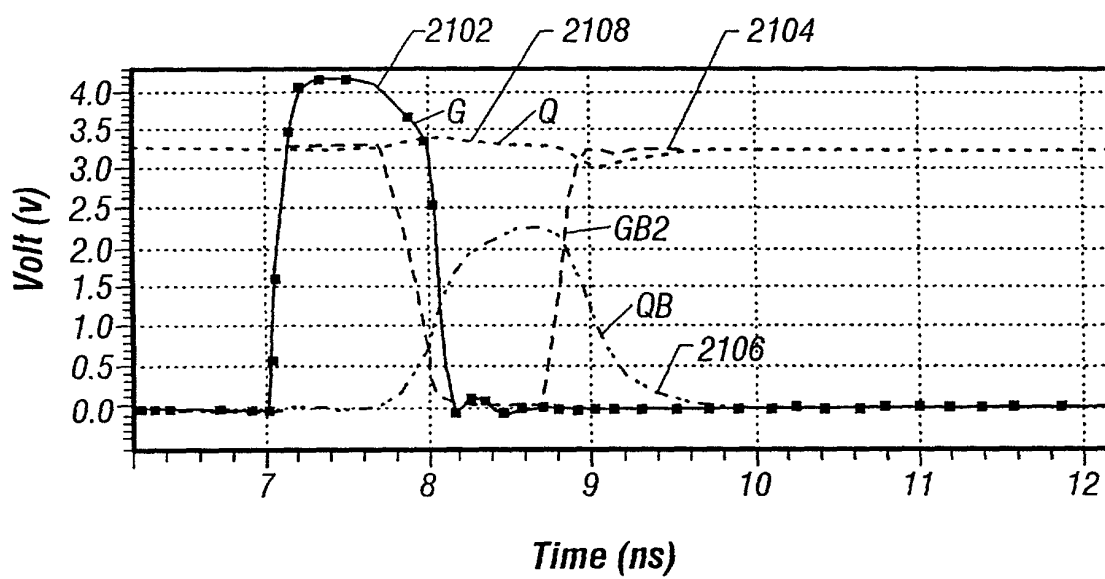


FIG. 21

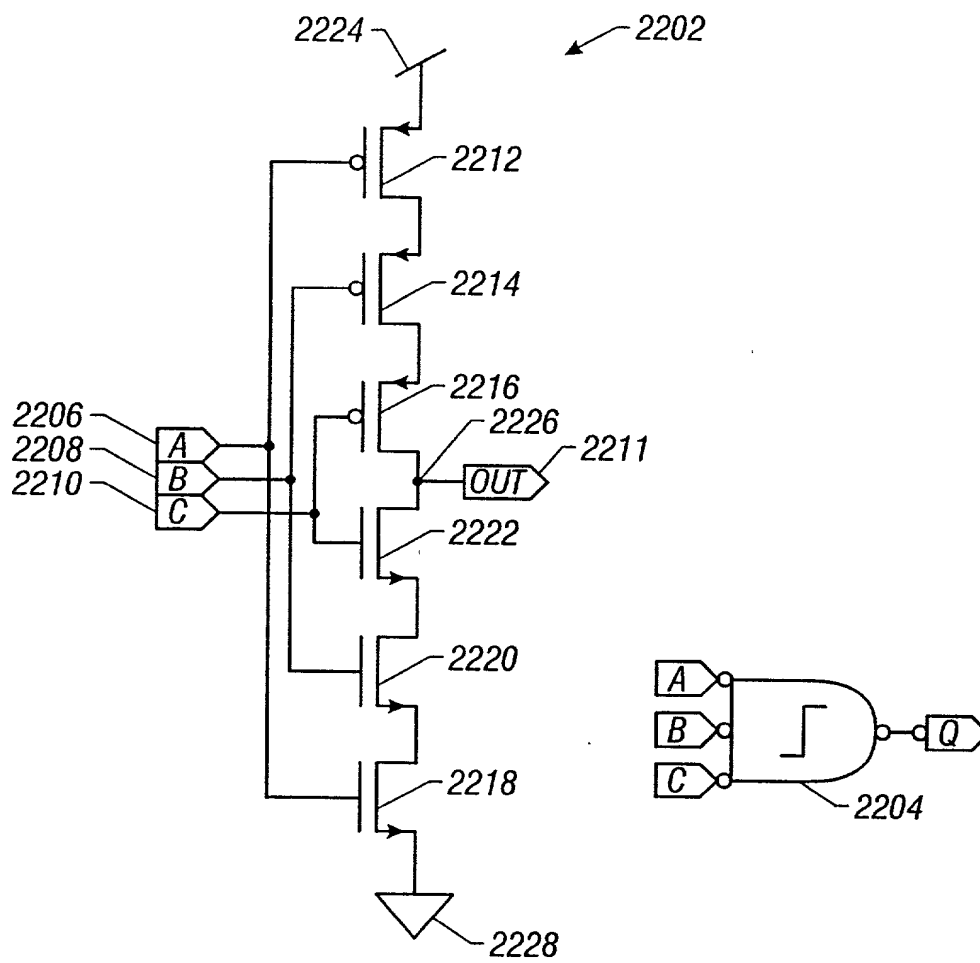


FIG. 22

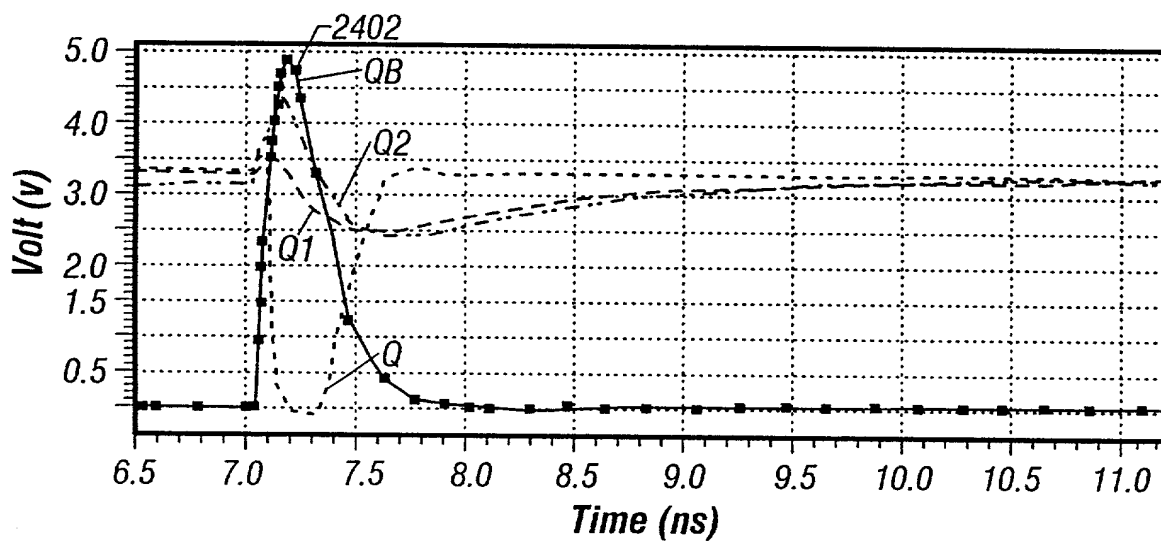


Figure 1 shows two schematic diagrams. The left diagram, labeled 2502, is a CMOS circuit. It features a PMOS transistor at the top with width $W=30*\lambda$ and length $L=2*\lambda$, and an NMOS transistor at the bottom with width $W=12*\lambda$ and length $L=2*\lambda$. The PMOS transistor's source is connected to a supply rail (indicated by a triangle symbol), and its gate is connected to input A. The NMOS transistor's source is connected to ground (indicated by a triangle symbol), and its gate is connected to input B. The drains of both transistors are connected to a common output node labeled OUT. The right diagram, labeled 2504, is a standard CMOS NAND gate. It has two inputs, A and B, and one output, OUT. The gate is represented by a rectangle with a 'J' shape inside, indicating a NAND function.

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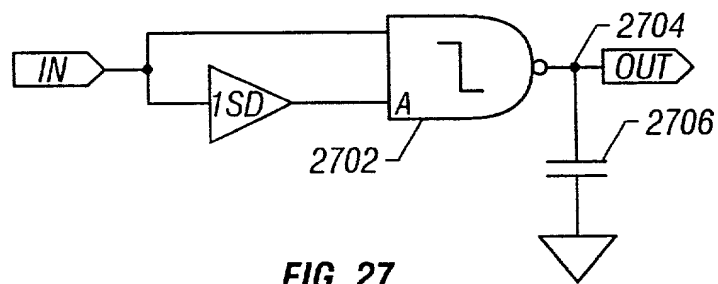


FIG. 27